REMARKS

The final Office Action dated January 3, 2005 has been reviewed and carefully considered. Claims 36-55 are pending. Claims 36-55 are rejected.

In paragraph three on page 2 of the Office Action, claims 36, 41-43, 48-50, and 53-55 were rejected under § 103(a) over Burkhardt, Jr. et al. (U.S. Patent No. 5,142,683) in view of Peterson et al. (U.S. Patent No. 6,665,673).

In paragraph four on page 5 of the Office Action, claims 37, 38, 40, 44, 45, 47, 51, and 52 were rejected under § 103(a) over Burkhardt, Jr. et al. (U.S. Patent No. 5,142,683) in view of Peterson et al. (U.S. Patent No. 6,665,673), and further in view of Suh et al. (U.S. App. Pub. No. 2002/0161536).

In paragraph 1 on page 6 of the Office Action, claims 39 and 46 were rejected under § 103(a) over Burkhardt, Jr. et al. (U.S. Patent No. 5,142,683) in view of Peterson et al. (U.S. Patent No. 6,665,673), Suh et al. (U.S. App. Pub. No. 2002/0161536), and further in view of Urui et al. (JP 61196613).

Applicant respectfully traverses the § 103(a) rejections. Applicant submits that the requirements for a §103(a) rejection are not present and a prima facie rejection fails because the Office Action fails to cite a reference or references that teach, disclose or suggest all the claim limitations of Applicant's Application.

Applicant's invention involves a host messaging unit for allowing asynchronous retrieval of a command from a host processor. The host messaging unit requires at least "a read controller, coupled to a bus, for determining when a host command has been provided to a host memory and for asynchronously retrieving the host command directly from a host memory via direct memory access; a validator, coupled to the read controller, for validating the retrieved host command; and a write controller, coupled to the bus, for asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access."

The Office Action stated that Burkhardt, Jr. et al. disclose memory 111 and service agent 121. The Office Action stated that service agent 121 acts as read controller and a write controller as recited in Applicant's claims. The Office Action admits that Burkhardt, Jr. et al. fail to

disclose that the host processor is bypassed. Nevertheless, the Office Action stated that Peterson teaches a validator to validate the request retrieval.

However, Appliant respectfully submits that Burkhardt, Jr. et al. merely disclose a type of *synchronous* communication protocol between processors or devices/agents. In Burkhardt, Jr. et al., a main processor includes common memory that is accessible by an auxiliary processor. Synchronization logic is used for synchronizing and controlling message communication among multiple processors connected to the work station system bus 27. Access to the system bus 27 is controlled by a circuit 60, which halts instructions or requests until the bus has been physically granted to the LAN interface module 16. To communicate, a sending processor interrupts the receiving processor which, in response to the interrupt, scans the mailboxes of common memory 111 to find the mailbox with its address therein thereby receiving the message.

Thus, Burkhardt, Jr. et al. fail to suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Rather, Burkhardt, Jr. et al. teach away from asynchronous communications via direct memory accessing by using an interrupt scheme which places a burden on the processors. This burden is exactly what Applicant's invention is designed to prevent.

In addition, Burkhardt, Jr. et al. fail to suggest that service agent 121 asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access. Rather, according to Burkhardt, Jr. et al., service agent 121 also requires circuit 60 to authorize access to the system bus 27.

Peterson et al. fail to remedy the deficiencies of Burkhardt, Jr. et al. Peterson et al. fail to disclose, teach or suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Peterson et al. also fail to disclose, teach or suggest asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access.

Still further, the alleged motivation for modifying Burkhardt, Jr. et al. with Peterson et al. is improper because the Office Action simply states the combination would enable "the system of Burkhardt to check for invalid commands and thus provide appropriate reaction." It is

respectfully submitted that the Office Action does not provide any evidence, nor is it apparent, that the Peterson et al. approach would be improved if the "Frame Invalid molecule" of Peterson et al. were to be included in the Burkhardt, Jr. et al. configuration. In fact, nowhere in Burkhardt, Jr. et al does it state invalid commands are of concern for the system and nowhere in Burkhardt Jr. et al does it state that it is desirable to check for invalid commands to provide an appropriate reaction. Furthermore, the Office Action provides no evidence to suggest those specific elements of Burkhardt, Jr. et al. that could be modified with elements of Peterson et al. Therefore, the § 103(a) rejection is improper as being conclusory, based on hindsight, and fails to show that the combination could be made with a reasonable likelihood of success. Applicant respectfully requests that the § 103(a) rejection of claims 36, 41-42, 48-50, and 53-55 be withdrawn.

Moreover, Peterson et al., Suh et al., and Urui et al., alone or in combination, fail to remedy the deficiencies of Burkhardt, Jr. et al. Peterson et al. merely teaches a frame invalid molecule. Suh et al. merely teaches a polling clock. Urui et al. merely teaches polling memory at a required time. However, Burkhardt, Jr. et al., Peterson et al., Suh et al., and Urui et al. alone or in combination, fail to disclose, teach or suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Burkhardt, Jr. et al., Peterson et al., Suh et al., and Urui et al., alone or in combination, also fail to disclose, teach or suggest asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access.

Therefore, Applicant respectfully submits that new claims 36-55 are patentable over the cited references and requests that the § 103(a) rejection of the claims be withdrawn.

Dependent claims 37-42, 44-49, and 51-53 are also patentable over the references, because they incorporate all of the limitations of the corresponding independent claims 36, 43, and 50. Further, dependent claims 37-42, 44-49, and 51-53 recite additional novel elements and limitations. Applicants reserve the right to argue independently the patentability of these additional novel aspects. Therefore, Applicants respectfully submit that dependent claims 37-42, 44-49, and 51-53 are patentable over the cited patent.

On the basis of the above amendments and remarks, it is respectfully submitted that the claims are in immediate condition for allowance. Accordingly, reconsideration of this

application and its allowance are requested. Please charge/credit Deposit Account No. 50-0996 (IBMS.040US01) for any deficiencies/overpayments.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Attorney for Applicant, David W. Lynch, at 651-686-6633 Ext. 116.

Respectfully submitted,

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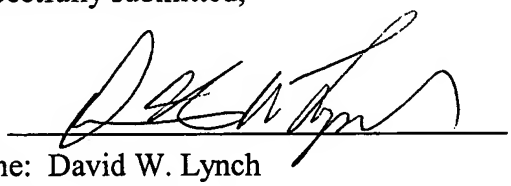
By: 
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